



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,646	02/27/2002	Theodore W. Houston	TI-28032.1	1358

23494 7590 06/18/2003

TEXAS INSTRUMENTS INCORPORATED  
P O BOX 655474, M/S 3999  
DALLAS, TX 75265

[REDACTED] EXAMINER

BERRY, RENEE R

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.  
10/085,646

Applicant(s)

Houston

Examiner

Renee Berry

Art Unit

2818



*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1)  Responsive to communication(s) filed on \_\_\_\_\_
  - 2a)  This action is FINAL.      2b)  This action is non-final.
  - 3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.
- Disposition of Claims**
- 4)  Claim(s) 18-36 is/are pending in the application.
  - 4a) Of the above, claim(s) 23-30 is/are withdrawn from consideration.
  - 5)  Claim(s) \_\_\_\_\_ is/are allowed.
  - 6)  Claim(s) 18-22 and 31-36 is/are rejected.
  - 7)  Claim(s) \_\_\_\_\_ is/are objected to.
  - 8)  Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9)  The specification is objected to by the Examiner.
- 10)  The drawing(s) filed on \_\_\_\_\_ is/are a)  accepted or b)  objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11)  The proposed drawing correction filed on \_\_\_\_\_ is: a)  approved b)  disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12)  The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13)  Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)  All b)  Some\* c)  None of:

1.  Certified copies of the priority documents have been received.
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\*See the attached detailed Office action for a list of the certified copies not received.

- 14)  Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).  
a)  The translation of the foreign language provisional application has been received.
- 15)  Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- 1)  Notice of References Cited (PTO-892)
- 2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3)  Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_
- 4)  Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5)  Notice of Informal Patent Application (PTO-152)
- 6)  Other: \_\_\_\_\_

Art Unit: 2818

## **DETAILED ACTION**

### ***Election/Restriction***

1. Newly submitted claims 23-30 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claims 23-30 are directed to an integrated circuit including a transistor while claims 18-22 and 31-36 are directed to an apparatus.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 23-30 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 18 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by US patent no. 5,589,412 to Iranmanesh et al.

In regard to claim 18, Iranmanesh teaches an apparatus having a semiconductor device which includes laterally spaced first and second sections with respective upwardly facing first and

Art Unit: 2818

second surfaces portions thereon; a third section projecting upwardly beyond each of the first and second surface portions from a location therebetween, the third section having two side surfaces on opposite sides thereof; an insulating layer which has portions disposed over the first and second surface portions, the third section extending into the insulating layer, and an insulating layer having first and second recess portions which respectively extend downwardly through the insulating layer toward the first and second surface portions on opposite sides of the third section, each of recess portion being immediately adjacent a respective side surface of the third section; a first portion of conductive material disposed in the first recess portion; and a second portion of conductive material disposed in the second recess portion at column 13, lines 58-67 to column 14, lines 1-60 (claim 1).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 19-22 and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent no. 5,589,412 to Iranmanesh et al. in view of US patent no. 5,360,757 to Lage.

Art Unit: 2818

In regard to claim 19, Iranmanesh teaches a semiconductor substrate having spaced source and drain regions which serve as the first and second sections, and including between the source and drain regions a gate section which includes a gate dielectric layer, a gate electrode over the gate dielectric layer, an insulator layer over the gate electrode, and insulator sidewalls on opposite sides of the gate dielectric layer, a gate electrode, and an insulator layer wherein the gate section is a third section at column 13, lines 58-67 to column 14, lines 1-60 (claim 1).

In regard to claim 20, Iranmanesh teaches first and second portions of conductive material have respective upwardly facing third and fourth surface portions thereon, the third and fourth surface portions being substantially coplanar with a top surface of an insulator layer at column 14, lines 6-22 (claim 1).

In regard to claim 22, Iranmanesh teaches side surfaces are spaced by a distance which corresponds to a minimum gate length in the semiconductor device at column 15, lines 23-25 (claim 6).

In regard to claim 31, Iranmanesh teaches the side surfaces of the third section have an insulator, insulator different from the substantially planar insulating layer at column 14, lines 6-22.

In regard to claim 32, Iranmanesh teaches the insulator is nitride and the substantially planar insulating layer is oxide at column 15, lines 23-25.

In regard to claim 33, Iranmanesh teaches a substantially planar insulating layer coplanar with the insulating layer covering the top portion of the control terminal wherein the control

Art Unit: 2818

terminal and the first and second terminals are within an opening in the substantially planar insulating layer at column 15, lines 23-25.

In regard to claim 34, Iranmanesh teaches the insulating layer covering the side portions and the top portion of the control terminal is nitride and the substantially planar insulating layer is oxide at column 14, lines 6-22.

In regard to claim 35, Iranmanesh teaches a substantially planar insulating layer coplanar with an insulating material covering the side and top portions of the gate stack wherein the gate stack and local interconnection terminals are within an opening in the substantially planar insulating layer at column 14, lines 6-22.

In regard to claim 36, Iranmanesh teaches an insulating layer material covering the side and top portions of the gate stack is nitride and the substantially planar insulating layer is oxide column 15, lines 23-25.

However, Iranmanesh does not teach the limitations of claim 21.

In regard to claim 21, Lage teaches an insulator layer includes alternating layers of a nitride and an oxide at column 5, lines 34-37.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Iranmanesh to include an insulator layer includes alternating layers of a nitride and an oxide, since such a modification is an art recognized substitute as described in column 5, lines 34-37 of Lage.

Art Unit: 2818

*Conclusion*

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. R. Berry whose telephone number is (703) 305-4544.



David Neims  
Supervisory Patent Examiner  
Technology Center 2800



RRB

April 7, 2003